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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/688,989	10/17/2000	Yoshitaka TSUNASHIMA	04329.1952-01000	2408

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EXAMINER	
RAO, SHRINIVAS H	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 12/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/688,989	TSUNASHIMA ET AL.	
	Examiner	Art Unit	
	Steven H. Rao	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 October 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *27,28 and 30-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *27-28,30-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Response to Amendment

Applicants' amendment filed on October 17, 2005 has been entered on October 21, 2005.

Therefore claims 1-15 and 18-33 as recited in the amendment are currently pending in the Application.

Claim Rejections - 35 USC Section 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:
A person shall be entitled to a patent unless -
(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in tie United States.

Claims 27 -28 and 30-34 are rejected under 35 U.S.C. 102(b) as being anticipated by De La Moneda et al. (U.S. Patent No. 4,445,267, herein after De La Moneda).

With respect to claim 27 De La Moneda describes a semiconductor device comprising: a semiconductor substrate including a first and second region separated by an isolation element , (De La Moneda figs. 1-1 # lo-substràte , figs. #12 isolation element col. 4 lines 20-25 etc.) a first transistor formed on the first region of the substrate (claim 7 , col. 6 lines 35-40) and including a first insulation film (figs. # 16 ,

and including a second insulation film and a second gate electrode arranged along the first direction, (figs. Structure above 18) wherein a side wall of the first gate electrode is connected to a side wall of the second gate electrode above the isolation element when viewed from a direction perpendicular to the first direction. (fig 10 # 42 connecting over isolation element 12).

With respect to claim 28, De La Moneda describes a device according to claim 33, wherein a side of the side insulator film is on a surface of said semiconductor . (De La Moneda figures e.g. fig. 10 #38 , col. 12-16) .

With respect to claim 30 De La Moneda describes a device according to claim 28, wherein at least one of said first and second gate electrodes is formed by a damascene gate process.. (De La Moneda figures 1-11 , same as Applicants' description at least at page 9 lines 10-25 and page 26 lines 2 to 20 for their gate formation) .

With respect to claim 31 De La Moneda describes a device according to claim 33, wherein said first insulation film is thinner than said second insulation film, said first transistor forms a logic circuit, and said second transistor forms a memory cell. (De La Moneda figures, col.2 lines 30-36).

With respect to claim 32 De La Moneda describes a device according to claim 33, wherein top surfaces of said first and second gate electrodes are coplanar. (De La Moneda figures).

With respect to claim 33 De La Moneda describes a device according to claim 27, wherein said second transistor further comprises a polysilicon layer formed on the

second insulation film formed on the substrate, (De La Moneda figure 10 # 20 over 16) and a side insulator film formed ùn a side of the second insulation film and a side wall of the polysilicon layer, (De La Moneda figure 10 # 38) said second gate electrode is formed on the polysilicon layer, (De La Moneda figure 10) and connected to the side wall of the second insulation film and the
side wall of the polysilicon layer via the side insulator film substrate. (De La Moneda figures specifically 10 and col. 6.,7).

With respect to claim 34 De La Modena describes a device to claim 27, wherein the side wall of the first gate electrode is directly connected to the side wall of the second gate electrode. (De La Modena figure 10 and see also Applicants' admitted prior art at least in figures 1-3E and the description at least page 6 lines 1-17 (especially 9-17).

Response to Arguments

Applicant's arguments filed on have been fully considered but they are not persuasive for the following reasons :

Applicants' contention is :

"Although the conductive layer 42 appears to connect the transistor devices in De La Moneda et al., layer 42 does not connect the side walls of the adjacent gate electrodes 20. In fact, insulating layers 38 cover the side walls of gate electrodes 20 such that these gate electrodes are not connected to each other physically or electrically. Therefore, De La Moneda et al. does not teach, at least, a side wall of the first gate electrode is connected to a side wall of the second gate electrode above the

isolation element when viewed from a direction perpendicular to the first direction, as recited in claim 27."

Applicants' above arguments are not consumarate with presently recited claims . The claims 27 (only independent claim) recitation, "a side wall of the first gate electrode is connected to a side wall of the second gate electrode above the isolation element when viewed from a direction perpendicular to the first direction" DOES NOT exclude De La Moneda's teaching (even according to Applicants') of the conductive layer 42 connecting with the side walls of adjacent gate electrodes , (OTHERWISE the conductive layer 42 will be not necessary and redundant) indirectly i.e with the presence of an insulating layer or without it .

If Applicants' want to distinguish De La Moneda from their presently recited claims they must amend the claims to recite "a side wall of the first gate electrode is DIRECTLY PHYSICALLY and without the presence of additional layers there between " connected to a side wall of the second gate electrode above the isolation element when viewed from a direction perpendicular to the first direction , or words to that effect that will clearly differenciate from the applied De LA Modena reference.

Alternatively , if Applicants' do not want change their claims , they have with draw this contention and show how the recited claim differs from the applied reference.

Applicants are reminded it is well settled law and accepted U.S. practice that Limitations from the specification cannot be relied upon since it is the language itself of the claims , which must particularly point out and distinctly claim the subject matter which the applicant regard as his invention, without limitations imported from the

specification, weather such language is couched in terms of means plus function or consists of a detailed recitation on the inventive matter. Limitations in the specification not included in the claim may not be relied upon to impact patentability to an otherwise unpatentable claim .

It also noted that Applicants' admitted PRIOR ART as shown at least in figures 1-3E and the description at least page 6 lines 1-17 (especially 9-17) shown both physical and electrical direct connection between element 16 and the first and second gates (including their side walls) and therefore Applicants' admitted prior art elements cannot form basis of distinguishing over prior art.

Therefore all of Applicants' arguments are not found persuasive and all pending claims i.e ONLY independent claim 27 and dependent claims 28, 30-33 and presently newly added claim 34 which repeats a part of the recitation, previously recited in claim 33 .

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven H. Rao whose telephone number is (571)272-1718. The examiner can normally be reached on 8.00 to 5.00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Fahmy Wael can be reached on (571) 272-1714. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Steven H. Rao

Patent Examiner

December 13, 2005.

LONG PHAM
PRIMARY EXAMINER